### EXP NO: 1 STUDY OF LOGIC GATES

1. **OBJECTIVES:**

To study about logic gates and verify their truth tables.

1. **TOOLS REQUIRED (MACHINES/EQUIPMENT/ACCESSORIES)**

|  |  |  |  |
| --- | --- | --- | --- |
| SL No. | COMPONENT | SPECIFICATION | QTY |
| 1. | AND GATE | IC 7408 | 1 |
| 2. | OR GATE | IC 7432 | 1 |
| 3. | NOT GATE | IC 7404 | 1 |
| 4. | NAND GATE 2 I/P | IC 7400 | 1 |
| 5. | NOR GATE | IC 7402 | 1 |
| 6. | X-OR GATE | IC 7486 | 1 |
| 7. | NAND GATE 3 I/P | IC 7410 | 1 |
| 8. | IC TRAINER KIT | - | 1 |

1. **PRE LAB WORK**
   1. **Theory / Definitions/ Formulas**

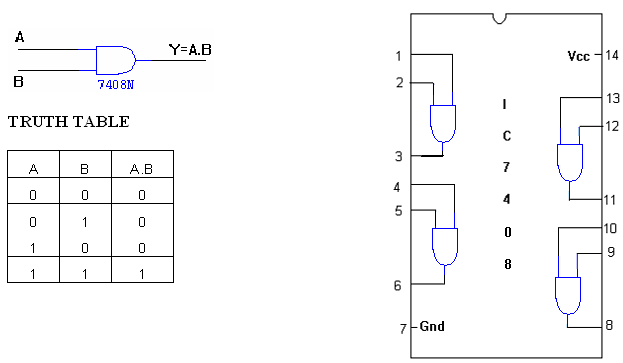
Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

**AND GATE:**

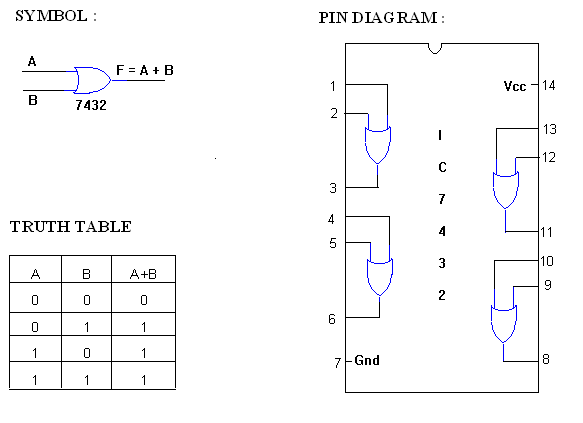
The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

**SYMBOL: PIN DIAGRAM:**



## OR GATE:

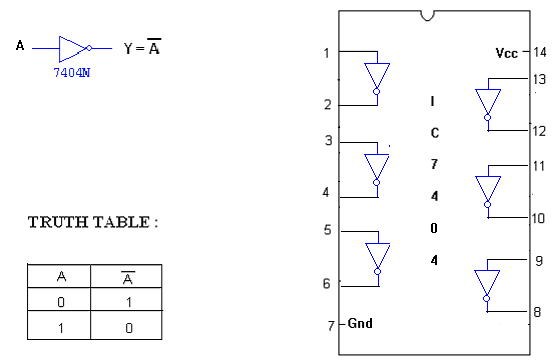
## The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.



**NOT GATE:**

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

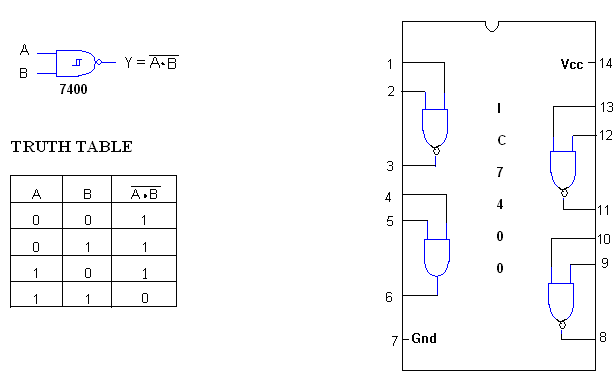
**SYMBOL: PIN DIAGRAM:**



**NAND GATE:**

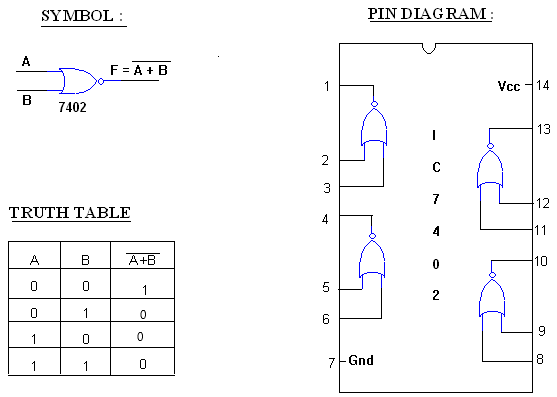
The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

**SYMBOL: PIN DIAGRAM:**

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**NOR GATE:**

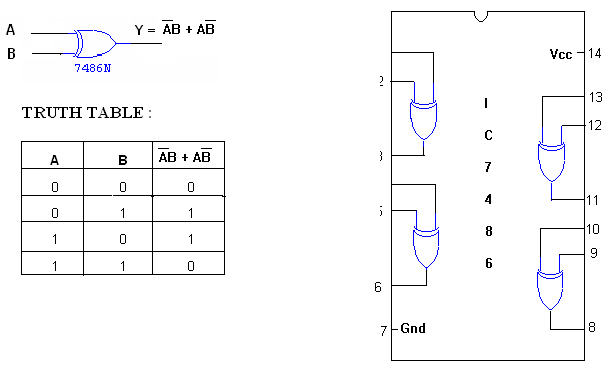
The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.



**X-OR GATE:**

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

**SYMBOL : PIN DIAGRAM :**

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* 1. **Experimental Procedure**

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.
4. **IN LAB WORK**

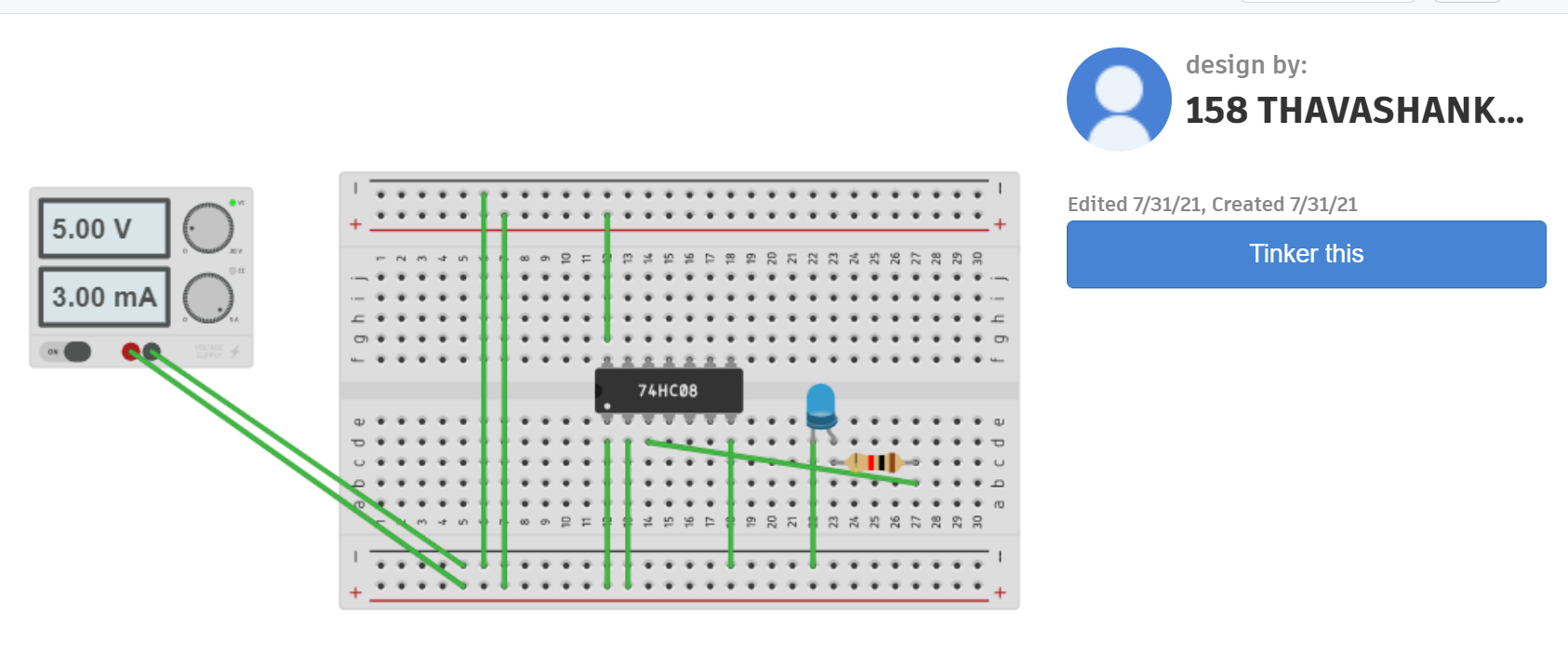
**4.1 Safety Instructions**

1. Follow all written and verbal instructions carefully.
2. Perform only those experiments authorized by your teacher.  Carefully follow all instructions, both written and oral.  Unauthorized experiments are not allowed.
3. Be prepared for your work in the laboratory.  Read all procedures thoroughly before entering the laboratory.
4. Observe good housekeeping practices.  Work areas should be kept clean and tidy at all times.
5. Dress properly during a laboratory activity.
6. A lab coat or smock should be worn during laboratory experiments.
7. Don’t work or connect with equipment while power supply is **ON** state.

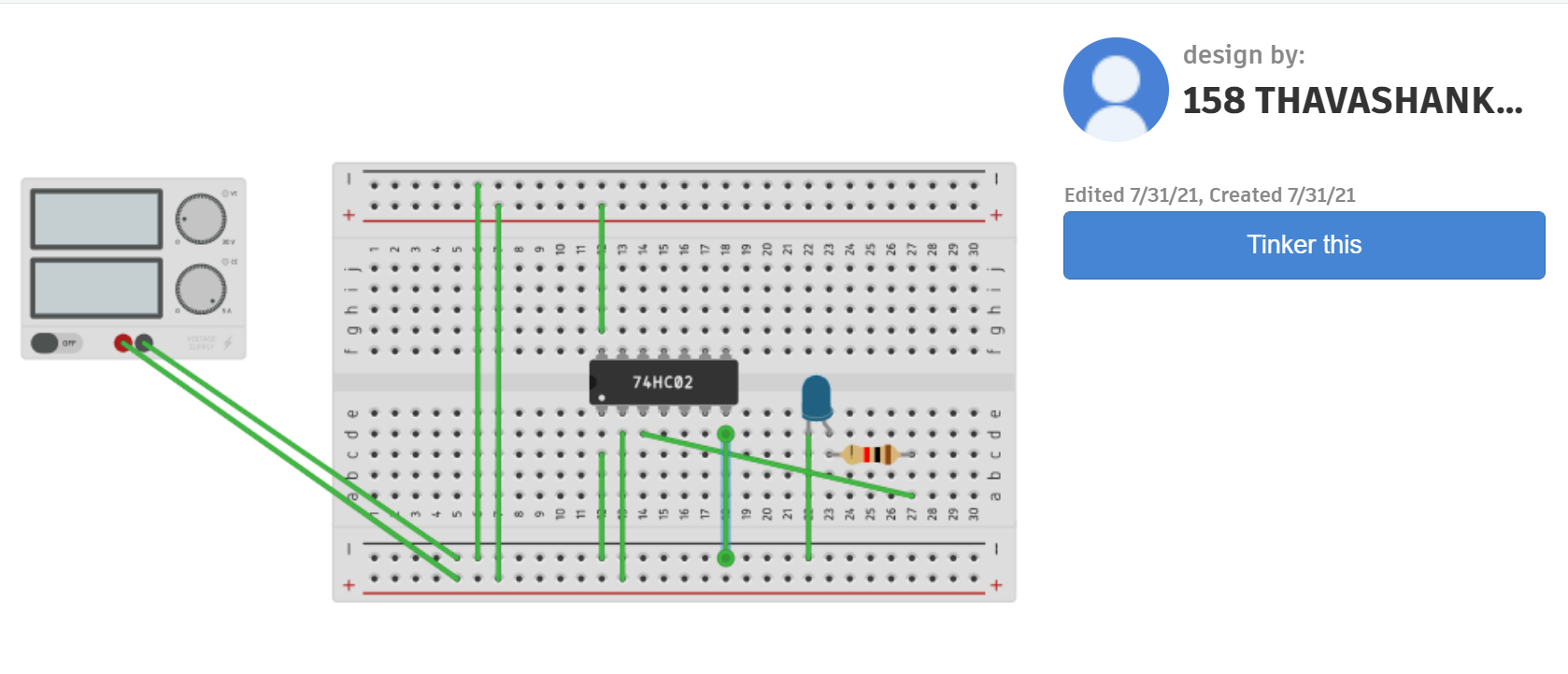
**4.2 Trouble shooting**

1. Check whether IC is working properly using the IC tester
2. Check for the loose connections in the circuit
3. Check for the short circuit in the connections.
4. Check for the correctness of the logic circuit.
5. **POST LAB WORK**

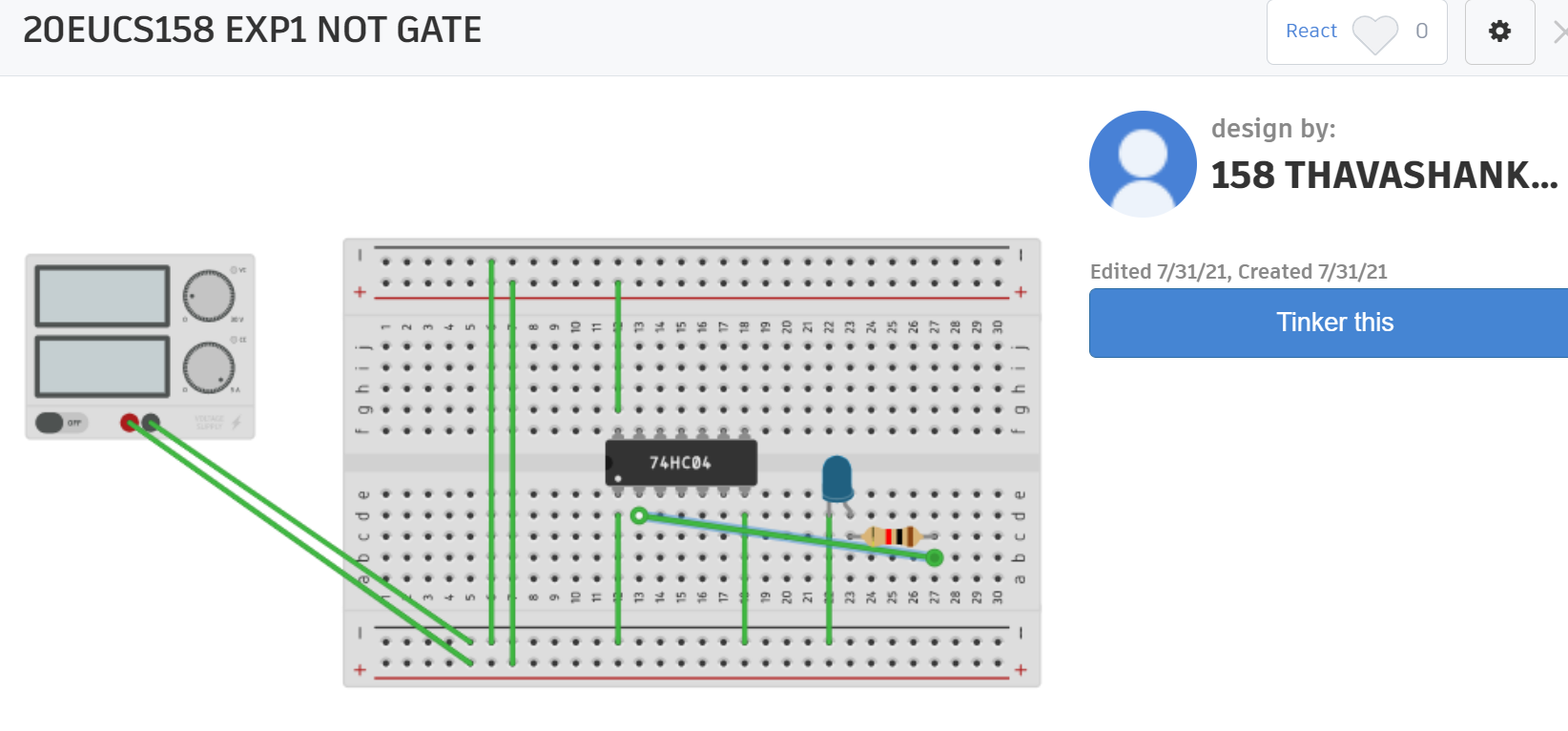
**AND GATE:**

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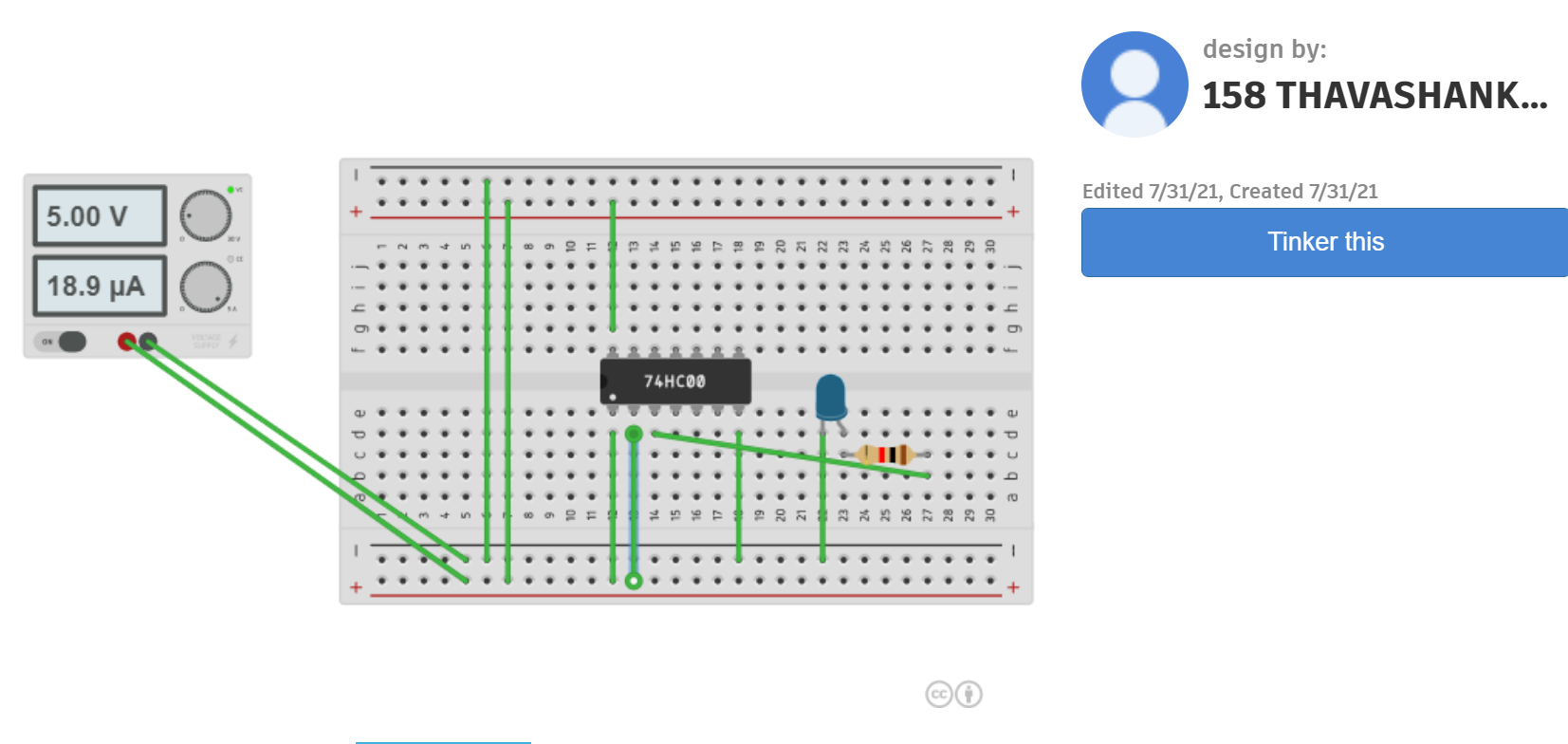
**OR GATE:**

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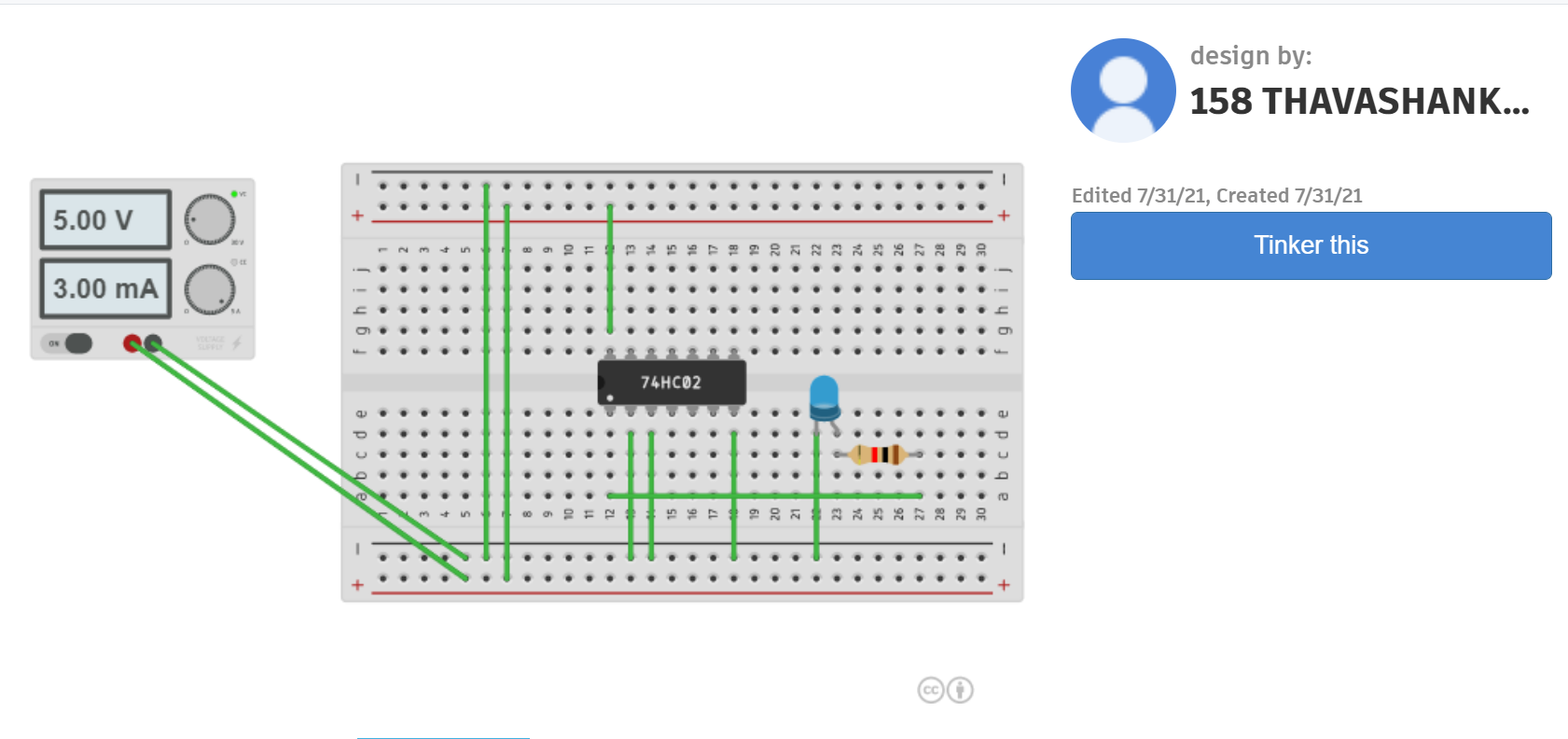
**NOT GATE:**

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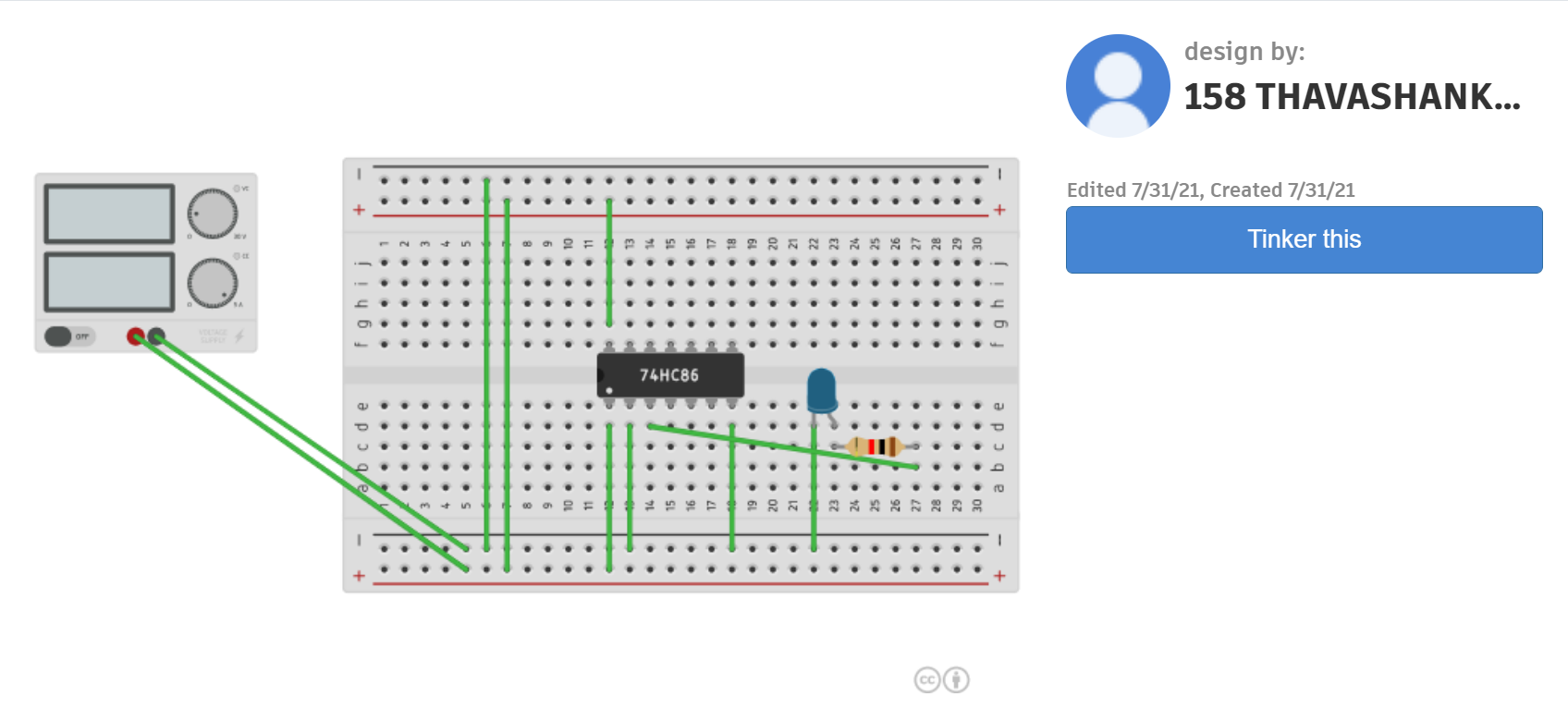
**NAND GATE:**

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**NOR GATE:**

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**XOR GATE:**

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**5.1 Result analysis**

Thus the logic gates were studied and their truth tables were verified.